PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-111420
(43)Dat of publication of application : 20.04.2001

(51)Int.Cl. H03L 7/18
H03L 7/10
H04B 7/26

(21)Application number : 11-283076
(22)Date of filing : 04.10.1999

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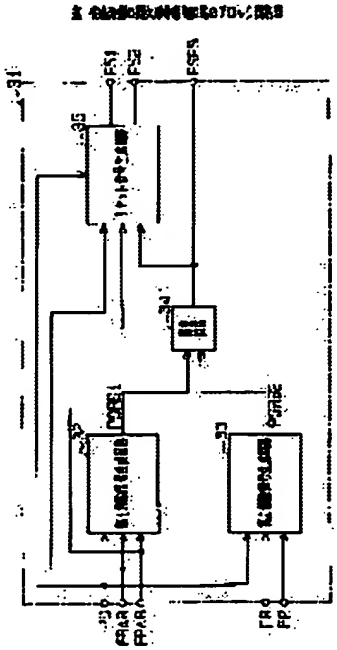
(54) INTERMITTENT OPERATION CONTROL CIRCUIT FOR PLL SYNTHESIZER

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a PLL synthesizer intermittent operation control circuit capable of quickly driving an internal circuit after resetting a power saving state.
SOLUTION: When a phase difference between a reference signal FRAR and a comparing signal FPAR falls within prescribed time, a 1st reset signal generation circuit 32 in the intermittent operation control circuit 31 generates a 1st internal power save reset signal PSRS1. A 2nd reset signal generation circuit 33 detects the output signal of a comparing frequency divider 22 or a reference frequency divider 23 and generates a 2nd internal power save reset signal PSRS2. A priority circuit 34 gives priority to an earlier signal out of the 1st and 2nd internal power save reset signals PSRS1, PSRS2 and generates a power save reset signal PSRS for resetting the power saving state of the internal circuit by the priority signal.



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[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision f rejecti n]

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